REMARKS

This is in response to the Office Action dated March 24, 2003. Claim 17 has been amended, and it is respectfully submitted that as amended all the pending claims are patentable.

35 U.S.C. 112, first paragraph

Claim 17 has been amended as above to overcome the rejection under 35 U.S.C. 112, first paragraph.

35 U.S.C. 103

In the Office Action dated March 24, 2003, the Examiner indicated:

"Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Pat. 6345502 to Tai et al. in view of US Pat.5618379 to Armacost et al. and further in view of US Pat 6033582 to Lee et al....

Tai teaches a method of forming a parylene membrance on a Si substrate (Fig. 1A-1F), ... Tai does not teach masking for deposition of a coating, or plasama etching to promote coating adhesion to a surface.

Lee et al. and indicated that Lee et al. teaches the modification of the surface of a substrate prior to coating. ... However it does not teach masking to prevent deposition of materials.

Armacost teaches the art of selectively masking a substrate to limit deposition of coatings from the vapor phase. ...

It would have been obvious to one of ordinary in the art at the time the invention was made to roughen the surfaces of substrate using a plasma etching, prior to coating a polymer film as taught by Lee and masking the protected areas of the substrate against deposition as taught by Armaxost while forming the parylene membrance on a Si support as taught by Tai because Lee teaches that the plasma etch produces distinctive surface morphologies which promote reliable and functional adhesion of materials to surfaces (4; 1-12) while Armacost teaches that deposit masking is conventional but in parylene coating the novel mask facilitates removal of the coating from undesired locations (1;38-44)"

Referring to Fig. 1A-1F, Tai teaches the steps of forming a SiO_2 layer on both surfaces of a Si substrate 100, and patterning the SiO_2 106 on the bottom surface to form a window 104. The Si substrate 100 exposed by the window 104 is then etched until the thinned silicon portion 112 is between 20 and 100 μm. The SiO_2 102 on the top surface is then removed, followed by deposition of parylene on both surfaces of the Si substrate 100. (Fig. 1A-1C, col. 2, lines 4-24).

It is known to the art that silicon removal rate of plasma etching can be as high as 20 μm every minute. If the thinned silicon portion 112 with the thickness ranged from 20 μm to 100 μm is further subjected to a plasma etching process prior to deposition of parylene, the whole thinned silicon portion 112 may easily be completely removed. In this manner, there will be no surface remaining at the window area for adhering the parylene layer, not to mention increasing the surface adhesion. Should one perform the plasma etching prior to the thinning step, the roughened surface will again be removed by the formation and removal of SiO_2.

Firstly, there is no suggestion or motivation for modifying Tai by incorporating the teaching of Lee et al.; and secondly, no reasonable expectation of success can be found by the teaching or suggestion for modification or combination proposed in the Office Action. Therefore, a *prima facie* case of obviousness has been established, and the rejection is respectfully traversed.

In addition, neither Tai nor Lee et al. teach the step "masking off a first surface of the metal substrate with a maskant, leaving a second surface of the metal substrate unmasked" as claimed in Claims 1 and 12. In Claims 1 and 12 of the present application, the first and second surfaces are two opposing surfaces of the metal substrate. Therefore, in this step, one of two opposing surface is covered by the maskant. However, as the objective of Tai is to deposit parylene on both surfaces of the silicon substrate 100 to increase the strength thereof. Should one apply a maskant on one of two opposing surfaces of the Si substrate 100, either the second parylene 130 cannot be formed, or the parylene 132 on the bottom surface for strengthening the edges 134 and 136 cannot be formed. Therefore, the proposed combination or modification of Tai, Lee et al. and Armacost renders Tai unsatisfactory for its intended purpose, which is to provide a strengthened parylene structure. This again proves that a *prima facie* case of obviousness has not been established.

The Office Action dated March 24, 2003 further indicated:

"Claims 1, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over International Pat. WO 01/022776 to Han et al. in view of the non-patent monograph of Licari et al. and further in view of US Pat. 3908075 to Jackson et al. and further in view of Armacost.

Han teaches the fabrication of a parylene diaphragm on a Si-substrate (fig. 3). The steps comprise depositing a parylene film (312) on one surface of the substrate followed by

patterning the backside of the substrate and etching the substrate to form a released diaphragm.

Han does not specifically list the steps of masking one surface, placing the substrate in vacuum, plasma etching the surface to be coated and coating the substrate in vacuum. ...

Patterning of substrate is conventionally carried out by photolithographic methods ...

The listed steps are conventional in a coating process and well known to one of ordinary skill in the art. This is shown by the monograph of Licari which teaches the use of parylene coatings in electronic applications (p.80-83), plasma cleaning of surfaces prior to coating (p.159-161) ...

Licari does not teach masking a surface before coating. Armcost teaches the conventional use of a mask to protect surfaces and as shadow masks (1;5-6;47)."

Han et al. teaches forming a parylene layer 308 on a ZnO layer 306 on one side of the substrate 302, and a parylene layer 312 covering Al electrode 310, where the thickness ZnO 306 is 0.5 μm, and the thickness of the Al electrode 310 is also 0.5 μm (Fig. 3A-3B, page 5, lines 10-18). As indicated by the Examiner, Han et al. does not teach the plasma etching for treating the unmasked substrate prior to deposition of parylene layer 312. As a matter of fact, all of the substrate surfaces have been masked by the SiN before depositing the parylene layer 312, there is no unmasked surface of the substrate to be treated. Therefore, Han et al. teaches away the step c "treating the unmasked second surface of the metal substrate by plasma etching" as claimed in Claims 1 and 12 of the present application. As there is no unmasked second surface of the metal substrate, even one ordinary skill in the art combine Han et al., Licari et al., Jackson et al. and Armacost, the teaching of treating the unmask second surface of the metal substrate is not disclosed unless one remove the Al electrode 310, the ZnO layer 306, and the Al electrode 304 prior to deposition of parylene to render Han et al. inoperative for its intended purpose. Therefore, firstly, Han et al, Licari et al., Jackson et al., and Armacost, individually or in combination, fails to teach every element as claimed in Claim 2; and secondly, the combination or modification of these cited references renders the principal reference Han et al. inoperative for its intended purpose.

In addition to the above, the parylene layer 312 is formed on the Al electrode 310 protruding from the parylene layer 308. Once the plasma etching is applied prior to deposition of parylene layer 312, the protruding Al electrode 310 is etched first. As the thickness of the Al electrode 310 is only 0.5 μm thick, a significant part will be easily

removed by only a few seconds of plasma etching. This may cause malfunction of the device. Therefore, there is not reasonable expectation of success for such modification.

Further, there shows no motivation or suggestion for modifying Han et al. by forming a maskant on one surface of the silicon substrate as disclosed in Armacost since all the surfaces of the silicon substrate have been covered by a silicon nitride layer already.

Therefore, as a *frima facie* case of obviousness has not been established, the rejection over Claims 1 and 12 is respectfully traversed.

Respectfully submitted,

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